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Research on High-Speed Data Collector of Blast Wave Signal Based on the Post-Trigger Principle

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Abstract: In view of the incomplete signal and other issues brought by the threshold trigger in the conventional blast wave signal test, this paper designed a post-trigger data high-speed collection method, adopted the ARM7 kernel MCU to complete the design of the hardware scheme and preparation of the corresponding test software, then developed the post-trigger data high-speed collector prototype, and completed the explosive shock wave signal collection through the test. Experiments show that the post-trigger high-speed data collector developed in this paper has the characteristics of simple interface circuit, high precision collection, good reliability, simple operation, which can meet the test requirements of blast wave.

Keywords: Blast wave signal, data sampling, post-trigged.

1. INTRODUCTION

Blast wave refers to a high-speed high pressure wave spread in the medium (air, water) after the explosion of the explosive, with the characteristics of high transmission speed, instance increase of the pressure on the surface of the wave, the signal test has been the difficulty of dynamic testing technology in weapons industry [1, 2]. Usually, the test of the blast wave test collection is conducted by high-speed data collection instrument, while testing, turn on the collection in advance and then record the way of blast wave signal, which usually will cause the problems of redundant data, difficult to find, increase data processing difficulty and the cost of hardware [3, 4]. But if the data are collected after the threshold signal is triggered, which usually may cause the problem of the incomplete tested waveform caused by the instantaneous uncollected waveform of the pre-trigger point. Other scholars have proposed some solutions, but there are the problems of circuit design complexity and high cost [5-7]. Therefore, This paper put forward a data collection instrument design principle based on the post-trigger data high-speed data collection, namely once the collector is turned on, it will be in the normal working state, then it conducts continuous high-speed sampling for the tested analog signal, when the trigger signal comes, it stops the collection after some delay, and then it records the signal at a certain time before and after the trigger point by setting to complete the collection and recording of the waveform of the whole shock wave. And design sampling hardware and major software programs according to the principle, and complete the development of the testing system prototype of the blast wave through the collection of the blast wave signal.

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2. DESIGN PRINCIPLES

Principles of high-speed data collection instrument are usually as follows: the collector is normally in a wait state and it begins sampling measurement only when trigger signal produced by the blast wave arrives. So the weaker the trigger signal of the effective trigger is, the closer the test signal is to the complete blast wave. After all, the blast wave goes before the trigger signal, so no matter how little the trigger signal will produce effective trigger, which cannot obtain the complete shock waves.

2.1. External Trigger Modes And Defects Of The Conventional Data Collection

In order to enable the external trigger signal to be effectively triggered, first of all, it is needed to set up a certain trigger condition, when the voltage of the input external trigger signal waveform exceeds the threshold voltage, it will produce the flip level of 0 to 1 or 1 to 0 to start the data collector to collect data.

External trigger signal is usually obtained through a trigger circuit [8]; a simple triggering circuit can be achieved by using a comparator, as shown in Fig. (**1**).

Trigger voltage threshold can be obtained by the partial pressure of dividing resistor R1 and the dividing resistor R2 to VCC, the supply voltage, the required trigger voltage threshold can be set by changing the resistance ratio of the dividing resistor R1 and the dividing resistor R2.

When the voltage of the input tested analog input signal (*i.e.* external trigger signal) is compared with the trigger voltage threshold, if the voltage of the analog signal is greater than the trigger threshold voltage, the external trigger signal output by the comparator changes from "0" to "1", the trigger signal occurs a valid triggering, that is, the trigger signal starts the collector to begin sampling [9, 10].

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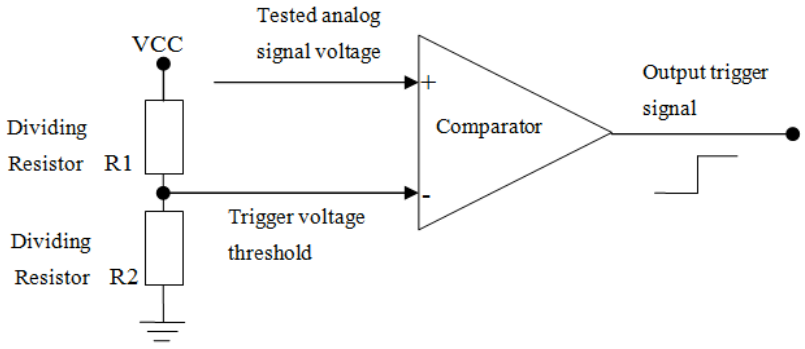

Fig. (1). Simple trigger circuit.

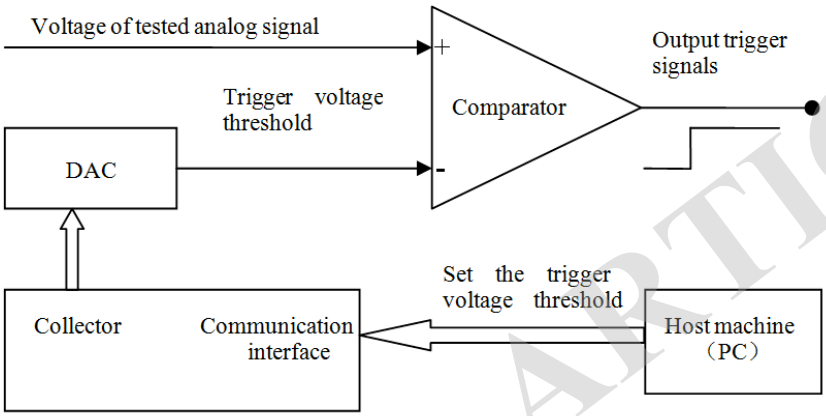

Fig. (2). Triggering circuit design with DAC.

In response to the uncertainty of the trigger threshold voltage in the actual test situation, a digital analog converter (DAC) can be used to obtain the trigger circuit design of the voltage threshold, as shown in Fig. (**2**).

General DAC receives the control and digital input on the host processor from the collector through data / address / control bus, or SPI bus receiver. After the digital quantity to achieve the corresponding required trigger voltage threshold is calculated, the background machine (PC) can send digital quantity to DAC through the UART communication interface to get the DAC output to trigger voltage threshold.

It can be seen that the method through the external trigger signal to start the collector sampling can only collect the waveform which the analog voltage signal is greater than the set threshold trigger voltage, so in order to measure the waveform signal of the complete blast waves as much as possible, it is needed to reduce the trigger voltage threshold as much as possible, but this will cause the occurrence of the false triggering [11].

2.2. Methods And Characteristics Of The Post-Trigger High-Speed Data Collection

Therefore, in view of the above problems, this paper designed a method of post-triggering high-speed data collection, namely with the same external trigger signal, not with the trigger starting the collector to begin sampling operation, but with the trigger causing the collector to stop sampling operation. At this time, the collector usually works in the normal condition, constantly monitoring the input tested analog signal and the external trigger signal. Once the collector is turned on, it will be in the normal working state, the tested continuous analog signal will be high-speed sampled, and the data collected are stored in the collector, being composed of RAM memory in FIFO. After the sampling time of ΔT, the sampling data stored in FIFO will automatically cover before the sampling data before the sampling time of ΔT. Assuming the capacity of FIFO is X bit, the collector uses the ADC of 16 bit precision, the sampling rate is Y MB / sec. ΔT can be calculated:

$$\Delta T = \frac{X}{16 * Y} \tag{1}$$

The test method of post-trigger high-speed data collection is as follows: the same external trigger signal is used to start a delay circuit, after the Δt delay of the circuit. A jump signal is generated to end the high-speed data sampling operation of collector. It can be seen that if Δt <ΔT, the sampling data in FIFO will not be covered; if Δt is greater than the time L cost from the beginning of the explosion to the end of the explosion, the collector will can completely collect the blast wave.

In practical design, the special delay circuit can be left out, and the external trigger signal can have direct access to some pin of the main processor, then the external trigger signal can start some timer of the processor, the time of the timer is set to be Δt. Then after the external trigger signal effectively starts the timer, the timer can interrupt after the Δt delay, high-speed sampling requesting the main processor to terminate the high-speed sampling operation of the collector.

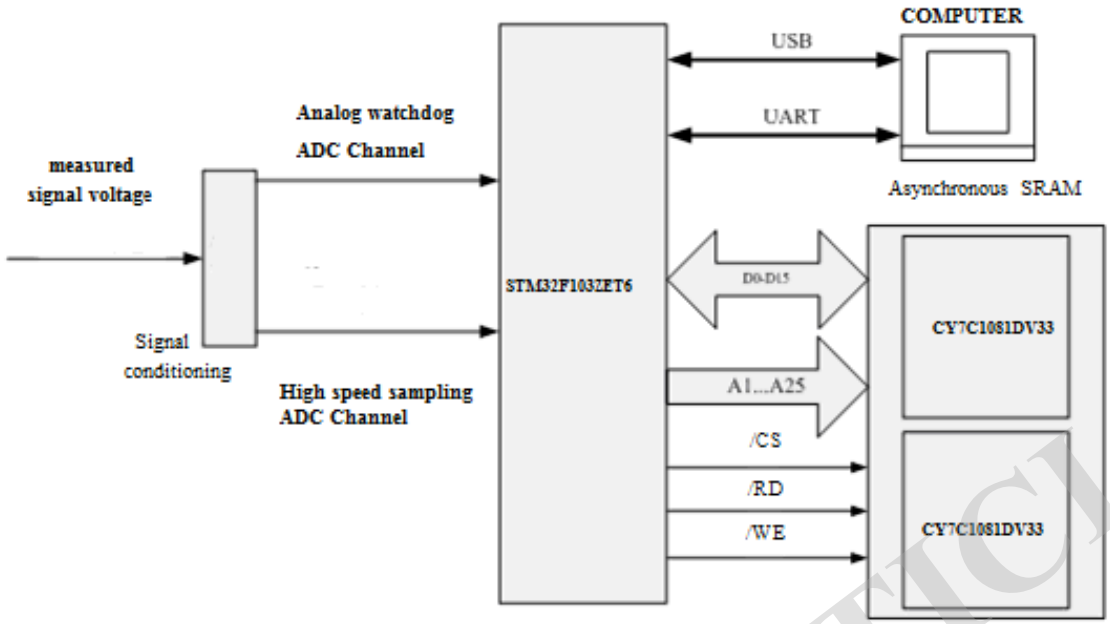

Fig. (3). Design diagram of hardware design of high-speed post trigger data acquisition.

3. HIGH SPEED SAMPLING OPERATION USED IN THE MEASUREMENT OF THE BLAST WAVE SIGNAL

3.1. Introduction To MCU Chip

The main processor adopted in this design is STM32F103ZET6, the processor is the enhanced MCU, 32 bit RISC kernel of the high-performance ARM Cortex-M3 is used, with the frequency of 72M, a built-in high-speed 512K-bytes flash memory and 64K-bytes SRAM, which has a wealth of I / O ports and functions. Including three 12-bit precision A / D converter ; 4 16-bit general timers; 2 PWM timers; it also has a variety of communication interfaces, including two I2C bus interfaces, three SPI interfaces, two I2S interfaces, an SDIO interface, 5 USART / UART interfaces, a USB interface and a CAN interface. Meanwhile, the chip also integrates a FSMC module, which has four chip selective outputs, which support PC Card / CF card, SRAM, PSRAM, NOR and NAND.

STM32F103ZET6 is built-in three 12-bit precision analog/digital converters (ADC). The maximum sampling rate is up to 1M. Each ADC shares up to 21 external channels, which can achieve single or scan sampling. ADC can achieve synchronous sampling and holding, cross sampling and holding, the logical control of a single sampling.

The built-in nested vector of STM32F103ZET6 interrupts the controller, which can handle up to 60 maskable interrupt channels and 16 priorities. Its external interrupt controller contains 19 edge detectors for generating an interrupt request. Each interrupt can be independently configured its trigger event (rising edge, falling edge or both edges), and can be individually shielded. There is a pending registers maintaining all of the interrupt request status.

STM32F103ZET6 has 26 address buses (AD0-AD25) and 16 data buses (D0-D15), and therefore, it can be extended up to 64M × 16 and an external SRAM.

3.2. Hardware Design

The overview of the working principle and hardware design of the high-speed post-trigger data collector using STM32F103ZET6 as the main processor is shown in Fig. (**3**). After the signal conditioning of the tested analog signal, trigger signal is separated and be input into the STM32 F103ZET6 analog sampling channel. STM32F103ZET6 achieves external RAM expansion *via* data /address /control bus. Fig. (**3**): Hardware Design Diagram of High-speed Post-trigger Data Collector.

As when the collector conducts high-speed data collection, the sampling data cannot be transmitted in real time, but chronologically stored inside the FIFO of the external SRAM. Only after the end of sampling, a host computer can be used (*i.e.* a PC in background services) to send commands to the collection *via* UART and other communication interfaces, taking the sample data existing in the RAM of the external collector.

3.3. Realization of The Function of Post-Trigger

The function of post-triggered of the collector can be realized by regarding one of the STM32F103ZET6 ADC channel to be simulated into watchdog, namely, one of ADC of the analog watchdog accurately monitors the external trigger signal, and the other ADCs collect the voltage of the selected and input analog signal. The workflow of the software is shown in Fig. (**4**).

When the external trigger signal monitored by the analog watchdog ADC exceeds a preset threshold, the STM32F103ZET6 will generate an interrupt signal to end the ADC sampling operation. An obvious advantage of such the ADC analog watchdog to monitor the external trigger signal is that it can conveniently precisely set the triggering voltage threshold according to the level of error of the actual external trigger signal, the sampling duration and anti-interference, accurate trigger voltage threshold setting of

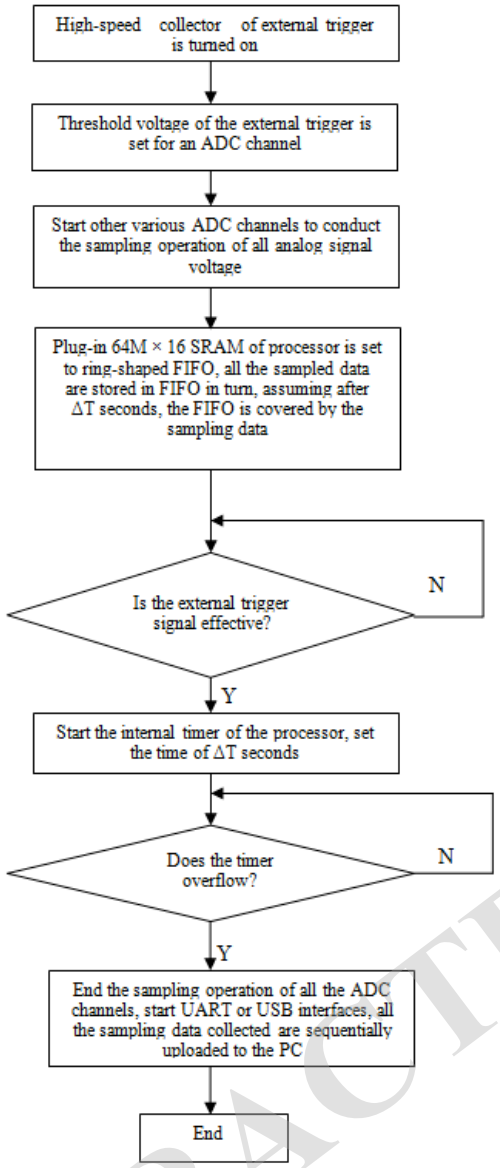

Fig. (4). Workflow diagram of the high-speed collector.

external trigger signal so as to facilitate the adjustment, be conducive to the collection of the sampling data of the complete waveform.

3.4. Design of External Expansion SRAM

Because the processor of STM32F103ZET6 is in-built with 12bit sampling accuracy of the ADC, and the data bus is 16 bits, so it can design the asynchronous SRAM according to the 16 bit data bus interface mode. STM32F103ZET6 has 64M external address space, therefore, the collector can be extended into 64M ×16bit external static SRAM.

But specifically, it can be determined how much the SRAM should be extended according to the actual size of the amount of sampling data, for example, in the collection of the signal voltage waveform of the tested explosion, the size of the external expansion SRAM can be determined according to the explosion duration and sampling rate. If the explosion lasts 5 seconds, the sampling rate is 500K and then the single-channel sampling requires only 2.5×16 Mbit external extension SRAM.

3.5. Main Functions of The Host Computer

The collector needs to have software installed on the host computer to complete the control of the behavior of the data collector and communication, data collection, storage, display, playback and other functions. And its control functions are described as follows:

Configure the comparison threshold of the external sampling trigger signal of the collector so that the external trigger signal can effectively trigger the processor in reaching the threshold voltage.

Set the time of ΔT of the delay sampling when the collector effectively trigger the external trigger signal so that the built-in ADC of the processor can stop the scheduled sampling time after of the triggering of the external trigger signal.

After the sampling, the host computer can send and upload commands of sampling data to the collector so that the collector will upload all the sampling data of the external SRAM to the PC.

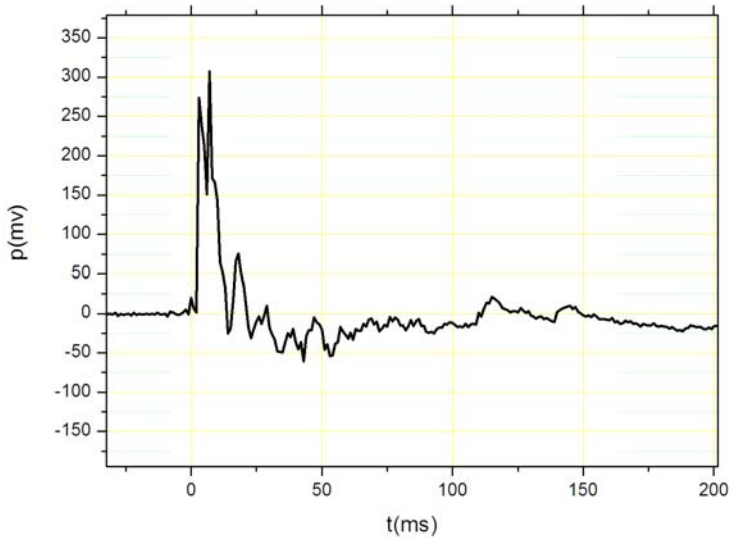

Fig. (5). Waveform figure of blast wave signal.

4. RESULTS

A set of post-triggers high-speed data collection was developed according to the above principles, and the blast wave signal of 10g TNT explosive was data sampled, setting the threshold trigger level is 20mv. The test results are shown in the following Fig. (**5**): in 0ms, the shock wave signal is 20mv(20kPa), in 8.5ms, the peak value of shock wave signal is 308mv(308kPa). If without the post-trigger function, the shock wave signal can be recorded only after 0ms, in this way, the shock wave signal is not complete. The high-speed data collector developed in this paper can completely record the waveform before 0ms; truly reflect the whole process of the explosion, which can meet the requirements of the blast wave test.

5. CONCLUSION

This paper used an ARM7 kernel MCU, developed a "post-trigger high speed data collector". The collector realized the functions of timely effectively and completely recording the explosion process by delaying the external trigger signal to end the working mode of the sampling process. And its interface circuit is simple with high precision, which is very suitable for the measurement of the explosion process, and has the widespread application prospect.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflict of interest.

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